# CESSON CONTRACTOR CONT

## Inrush limiter also provides short-circuit protection

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For containing large amounts of bulk capacitance, controlling inrush currents poses problems. The simplest approach involves placing an inrush-limiting resistor in series with the capacitor bank, but a resistor wastes power and adds a voltage drop. The circuit in Figure 1 addresses these problems and provides an additional benefit. At start-up, bipolar PNP transistor Q, holds N-channel power MOSFET transistor  $Q_1$  off until the voltage across capacitor  $C_1$  reaches a high enough level to turn off Q<sub>2</sub>. During this interval, resistor  $R_1$  supplies  $C_1$  and the rest of the circuit with start-up current. When  $Q_2$  turns off,  $Q_1$  turns on and provides a low-resistance path across  $R_1$ . When you shut off external power, the circuit resets as C<sub>1</sub> discharges.

As an additional benefit, this circuit provides protection against short-cir-

cuited loads. As current through  $Q_1$ increases, the voltage drop across  $Q_1$ increases due to Q<sub>1</sub>'s internal on-resistance. When the voltage drop  $across Q_1$ reaches approximately 0.6V (Q<sub>2</sub>'s  $V_{BE(ON)}$  voltage),  $Q_2$  turns on, turning off  $Q_1$  and forcing load current through R<sub>1</sub>. Removing the short circuit restores normal operation, allowing Q<sub>2</sub> to turn off and  $Q_1$  to turn on. Note that, because Q<sub>1</sub>'s on-resistance acts as a current-sense resistor for this function, the short-circuit trip point may vary depending on ambient temperature and  $Q_1$ 's characteristics. You can adjust  $Q_1$ 's turn-on and -off threshold by selecting  $R_1$  and  $Q_1$ 's on-resistance characteristic. Adding a conventional or zener diode in series with  $Q_2$ 's emitter increases the short-circuit trip current.

The components and values for constructing this circuit depend on the



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application. Depending on the design requirements, you may need to select a high-power resistor for  $R_1$  or add a heat dissipater to  $Q_1$ , but, for many applications, the circuit saves power over a conventional approach.**EDN** 

#### Microprocessorbased dual timer features four outputs

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Based on Freescale Semiconductor's MCC908QY 8-bit flash-memory microcomputer, the circuit in Figure 1 provides a low-cost, general-purpose dual timer that offers an alternative to one-shot circuits. You can modify the assembly-language software available from the online version of this Design Idea at www.edn.com/050609di2 to meet specific applications. The circuit uses microprocessor IC<sub>1</sub>'s internal 12.8-MHz clock oscillator. Internal division by four yields 3.2 MHz, which further divides by 64 with a timer prescaler to produce 50 kHz. A timer modulo counter divides by 50,000 to produce a 1-Hz timebase that generates a once-per-second real-time interrupt and master timing interval.

Two groups of four switches,  $S_3$  through  $S_6$  and  $S_7$  through  $S_{10}$ , set time intervals  $t_1$  and  $t_2$ , respectively, in increments of 1 to 16 sec. Although the **figure** shows individual DIP switches, you can also use hexadecimal-encoded rotary switches to set the





time intervals. For demonstration purposes, LEDs  $D_1$  through  $D_4$  show the outputs' states during the timing cycle. Normally open pushbutton switches  $S_1$ 

and  $S_2$  start and stop the timers' operating cycles. The start function initiates the main timer and operates only when the timer stops. After activation, out-



put  $Q_1$  goes to logic one during interval  $t_1$  (**Figure 2**). Output  $Q_2$  complements  $Q_1$  and remains at logic one until the next cycle starts. On  $Q_1$ 's trailing edge, output  $Q_3$  goes to logic one for time interval  $t_2$ . After  $t_2$  elapses, output  $Q_4$  goes to logic one and remains there until the next cycle starts. You can use the stop switch,  $S_2$ , at any time to terminate a cycle and reset all four outputs to logic one.EDN

#### Wide-range voltage regulator automatically selects operating mode

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The circuit in Figure 1 delivers programming voltages to an EEPROM under the control of an external DAC (not shown). You can replace the DAC with a potentiometer to create a general-purpose power supply operating from 12V and able to deliver a variable output voltage of 0 to 32V. As Figure 1 shows, a Linear Technology LT1072HV variable-boost switching regulator, IC<sub>1</sub>, drives a Class A amplifier comprising operational amplifier  $IC_2$ , voltage-boost-stage  $Q_3$ , and emitter-follower Darlington transistor  $Q_2$ . Resistors  $R_9$  and  $R_{10}$  set the amplifier's noninverting loop gain to a value of  $1 + (R_0/R_{10})$ .

For output voltages below 8V, switching regulator IC<sub>1</sub> remains in shutdown mode, and the output stage draws current through L<sub>1</sub> and D<sub>1</sub>. Q<sub>1</sub>'s collector voltage, V<sub>C</sub>, measures approximately 11.4V—that is, 12V minus D<sub>1</sub>'s forward-voltage drop. Transistor Q<sub>1</sub> monitors the voltage drop across R<sub>7</sub>, which measures a fraction of Q<sub>2</sub>'s collectorbase voltage, V<sub>CB</sub>. As long as V<sub>CB</sub> exceeds 1V, Q<sub>1</sub>'s collector current remains high enough to drive IC<sub>1</sub>'s feedback input higher than 1.25V, which in turn keeps IC<sub>1</sub> shut down.

As the output voltage increases, the voltage differential across  $R_7$  decreases, and, when it drops below 0.9V,  $Q_1$ 's col-

lector current decreases, lowering the feedback voltage applied to  $IC_1$  and switching it on. The boost regulator's output voltage increases, and the  $Q_1$ - $IC_1$  feedback loop regulates the collector-emitter voltage differential across  $Q_2$  to a constant 3V for all outputs exceeding 8V. If  $IC_2$ 's output goes to ground, cutting off  $Q_3$  and forcing  $Q_2$  into saturation, the feedback loop around  $Q_1$  opens and allows the circuit's output voltage to increase. Diode  $D_5$  and associated components form an overvoltage-protection clamp that limits  $IC_1$ 's output to 37V.

Resistive divider  $R_9$  and  $R_{10}$  and  $IC_2$  determine the output voltage's range.

Apart from selecting the  $V_{CE}$  ratings of  $Q_1$  and  $Q_3$  to withstand the highest desired output voltage, values of other

components are not critical. If you substitute appropriate components for  $D_5$ , Q<sub>1</sub>, and Q<sub>3</sub>, the circuit can deliver out- LT1072HV variant—minus 3V.EDN

put voltages as high as IC,'s maximum output-switch rating-75V for the



Figure 1 Able to deliver a wide range of output voltages, this regulator circuit automatically selects a linear or a switched mode as required.

### CMOS hex inverter generates low-distortion sine waves

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This Design Idea provides a simple, inexpensive, portable circuit as an alternative to a microcontroller to provide a wide-range source of lowdistortion sine waves for audio-circuit design and debugging. Although sine waves from DDS (direct digital synthesis) offer greater stability and fewer harmonics and other spurious-frequency components, this more "retro" approach lets designers use Linear Technology Corp's LTSpice freeware and hone their circuit-simulation skills. An oscillator comprises a frequency-determining network and a

method of limiting oscillation amplitude to prevent circuit saturation, waveform clipping, and the generation of harmonics. Many audio-oscillator designs use classic Wien-bridge bandpass-filter topology and include incandescent lamps, thermistors, or JFET circuits as amplitude-sensitive resistors to automatically vary feedback and limit amplitude.

However, amplitude-sensitive resistors introduce a small delay that can cause amplitude ringing while the oscillator stabilizes. In addition, the limiter's "soft" characteristics require frequency-determining components that track closely and maintain a level amplitude response over the oscillation range. Diode limiters present a softer characteristic than allowing an amplifier to go into "hard" limiting, and a diode limiter introduces no envelope delay. A Wien-bridge filter's frequency response rolls off relatively slowly and thus inadequately rejects clipping-induced harmonic frequencies. As a consequence, designers of most high-quality oscillators eschew the use of hard-clipping limiters.

Figure 1 shows a sine-wave-oscilla-



tor design that makes unconventional use of a logic circuit. Based on statevariable topology that provides buffered highpass-, bandpass-, and lowpass-filtering nodes in one circuit, this oscillator relies on the peaking characteristics of an underdamped, two-pole lowpass filter that significantly boosts response at the fundamental frequency. In addition, the filter's lowpass node provides -12-dB-per-octave attenuation for harmonics. The state-variable loop comprises two integrators and a summing amplifier that provides 180° of phase shift. The two integrators each add almost  $-90^{\circ}$  of additional phase shift, and the whole loop thus presents slightly less than 360 or 0° of phase shift and unity gain for oscillation.

The loop's gain blocks comprise un-

buffered 74HCU04 CMOS inverters that emphasize circuit simplicity, wide bandwidth, and self-referencing logic thresholds. Individual inverters each provide relatively low-voltage gains of approximately 15 per stage. Operating in Class A linear mode, the inverters produce no crossover distortion and thus produce harmonic amplitudes that decrease rapidly with harmonic order. In addition, a 74HCU04 package contains six inverters, making possible a one-device oscillator circuit.

To understand how the circuit operates, use the summing node at  $IC_{1C}$ 's input as a phase reference. Summing amplifier  $IC_{1C}$  provides the first 180° of phase shift (inversion). Inverter/integrators  $IC_{1A}$  and  $IC_{1B}$  each present a quality factor, Q, equal to a gain of approximately 15, contributing a phase shift of  $-86^{\circ}$  for a total of  $180-86=94^{\circ}$  each. The total phase margin for the three stages is  $180+94+94=8^{\circ}$  degrees. The circuit's phase shift now amounts to 8° away from the "perfect" 0° phase required for oscillation. The total circuit Q of approximately 7.5 provides a boosted fundamental-frequency-filtering action of approximately 17 dB, but, at 8° phase shift, the circuit does not oscillate.

To obtain the exact  $360^{\circ}$  phase shift for oscillation, apply a small amount of signal from the filter's bandpass tap, which operates at a phase angle of  $180+180-86=-86^{\circ}$ . Combine the circuit's Q of 7.5 and attenuate the bandpass intermediate output's signal at the bandpass filter by a factor of four,

and the circuit oscillates with adequate gain and phase margins. Due to its symmetric internal configuration, a CMOS-inverter circuit attempts to maintain a logic threshold of one-half of its supply voltage. However, an Nchannel MOS transistor conducts more than its P-channel counterpart, and the logic threshold shifts slightly toward the negative supply rail. Because an imbalance would lead to asymmetry if you use it as is for limiting the oscillation's amplitude, a pair of back-to-back 1N4148 diodes, D1 and D<sub>2</sub>, serves as a symmetrical limiter, preventing the gates from clipping the bandpass filter's output.

Soft clipping eases the filter's performance requirements by producing a third-harmonic level of -17 dB at the clipper's output. The filter's response peaks at 17 dB at the oscillation frequency, and the lowpass node provides 20 dB of third-harmonic attenuation for a theoretical third-harmonic total rejection of -54 dB. In practice, the CMOS devices' gain and threshold characteristics depart from ideal performance, and, as a result, the circuit produces sine waves that approach 1% distortion at the lowpass node, an acceptable level for the intended application. Replacing the CMOS inverters with operational amplifiers would further enhance performance.

The filter's highpass node provides the first integrator's input signal, and the two cascaded integrators approach a 180° phase shift for all frequency components and also attenuate harmonic frequencies by a factor of  $1/N^2$ , where N represents the harmonic number. Subtracting some of the highpass signal, which contains harmonics produced by the diode limiter, from the lowpass signal further reduces the output's harmonic components. Resistors R<sub>o</sub> and R<sub>o</sub> form a 10-to-1 cancellation circuit that provides an additional 6-dB harmonic reduction for a 0.5% distortion figure at the signal output. Figure 2 shows harmonic levels for a 500-Hz fundamental output frequency.

Oscillation occurs at unity gain at which the integrator's capacitive reactance equals the integrator's resistance,



Figure 2 The oscillator's output spectrum contains second- and third-harmonic levels of at least 250 dB below the fundamental.

and at a frequency of  $1/(2 \times \pi \times R \times C)$ , where  $R = (RV_1 + R_2) = (RV_2 + R_3)$ , and  $C=C_1=C_2$ . For C=10 nF and values of R of 8 to 80 k $\Omega$ , the circuit produces frequencies of 200 Hz to 2 kHz. You can use a 100-k $\Omega$ , dual-section ganged stereo-audio potentiometer as a frequency control. The control's ganged sections ensure that the integrators' resistance elements adequately track each other. To cover the audio spectrum of 2 Hz to 200 kHz, add a twosection band switch (not shown) to select pairs of capacitors with values of 1 µF, 100 nF, 10 nF, 1 nF, and 100 pF. You can use matched pairs of temperature-stable ceramic capacitors, but film-dielectric capacitors improve frequency stability. Compensation capacitor C3 improves output flatness at higher frequencies. Over a typical frequency band, the output amplitude remains flat within 1 dB.

One of  $IC_1$ 's three remaining inverters,  $IC_{1F}$ , serves as a virtual-ground generator by dividing the 5V power supply, a floating four-cell stack of AAsized nickel-cadmium or nickel-metalhydride batteries. Current drain from the batteries averages 50 to 60 mA. Switch S<sub>1</sub> connects the remaining inverters,  $IC_{1D}$  and  $IC_{1E}$ , to form a unitygain buffer amplifier for sine-wave outputs or as a Schmidt trigger to produce a square-wave output. Resistor  $R_{11}$  sets the Schmidt trigger's hysteresis level. For ease of construction, use a perforated prototype board and the DIP version of the 74HCU04.

When you construct the circuit, note that the 74HCU04 can deliver appreciable gain at high frequencies, and excessively long leads can provoke parasitic oscillations that resistor  $R_1$  helps suppress by reducing gain at frequencies in the very-high-frequency range. If you reduce circuit values, this oscillator easily operates in the high-frequency range, and, although its stability doesn't approach that of an LC-based oscillator, the circuit offers easy adjustment over a wide frequency range.EDN

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